IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Hisashi Ohtani et al.	Art Unit	: 2815
Serial No.	: 09/379,702	Examiner	: Eugene Lee
Filed	: August 24, 1999	Confirmation No.:	1613
Title	: METHOD OF FABRICATING SEMICONDUCTOR DEVICES		

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SUBSTITUTE BRIEF ON APPEAL

In response to the notice from the Examiner dated October 19, 2005, applicant submits the attached substitute brief on appeal. This substitute brief is in compliance with 37 CFR 41.47.

(1) Real Party in Interest

Semiconductor Energy Laboratory Co., Ltd., the assignee of this application, is the real party in interest.

(2) Related Appeals and Interferences

There are no related appeals or interferences.

(3) Status of Claims

Claims 45-64 are pending in this application, with claims 45-49 being independent. The claims have been rejected as being unpatentable over Yamazaki (U.S. Patent No. 5,315,132) in view of Matsumoto (U.S. Patent No. 5,396,084).

(4) Status of Amendments

The claims have not been amended subsequent to the final rejection dated February 4, 2004. A Notice of Appeal was filed on July 6, 2004. Appellant notes that the amendment of July 16, 2003, included a typographical error that inadvertently introduced a second claim 46 and renumbered claims 46-49 as 47-50 (though not in the form of an amendment). The listing of claims below corrects this error.

(5) Summary of Claimed Subject Matter

The claimed subject matter is directed to semiconductor devices that include a crystalline semiconductor island and a gate insulating film that includes first and second insulating films. The following summarizes each independent claim with references to the application specification and drawings. The references to the specification and drawings are meant to be exemplary, and not limiting.

With reference to Figs. 2A-2D, independent claim 45 is directed to a semiconductor device that includes a crystalline semiconductor island comprising silicon over a substrate 101 and including a source region 113, a drain region 114 and a channel formation region 115 provided between the source and the drain region. See page 16, lines 5-14. The device also includes a gate insulating film 110 and a gate electrode 111 over the gate insulating film. See page 15, lines 9-25. The gate insulating film includes a first insulating film 104 over the crystalline semiconductor island and a second insulating film 109 over the first insulating film. See page 15, lines 2-8. The first insulating film has a side aligned with a side of the crystalline semiconductor island, and the second insulating film extends beyond an edge of the first insulating film. See Figs. 2A-2D.

Independent claim 46 is directed to a semiconductor device that varies from the device of claim 45 in that claim 46 recites that the insulating films comprise silicon oxide. See page 15, lines 2-8. Similarly, independent claims 47-49 recite arrangements in which the first insulating film comprises silicon oxide and the second insulating film comprises silicon nitride (claim 47); the first insulating film comprises silicon nitride and the second insulating film comprises silicon oxide (claim 48); and the first and second insulating films comprise silicon nitride (claim 49). See page 15, lines 9-17.

(6) Grounds of Rejection to be Reviewed on Appeal

Claims 45-64 have been rejected as being obvious over Yamazaki (U.S. Patent No. 5,315,132) in view of Matsumoto (U.S. Patent No. 5,396,084).

(7) Argument

The subject matter of claims 45-64 would not have been obvious over Yamazaki in view of Matsumoto.

Appellant submits that an impermissible hindsight reconstruction of the invention is used to combine Yamazaki and Matsumoto in order to reject the claims, and requests reversal of the rejection for at least this reason. In particular, appellant believes that such impermissible hindsight is used in combining Yamazaki and Matsumoto to obtain the recitation in each of the independent claims that the first insulating film has a side aligned with a side of the crystalline semiconductor island, and that the second insulating film extends beyond an edge of the first insulating film.

Yamazaki shows a gate insulating film 3 that is 0.1 mm thick (see col. 6, line 21, noting a thickness of 1000 Angstroms) and is aligned with a side of a semiconductor crystalline island that is 0.7 mm thick (see col. 6, line 12). A gate electrode that is 0.3 mm thick (see col. 6, lines 22-26) is formed on the gate insulating film.

Matsumoto shows a circuit in which the gate electrode 20 of a NMOS thin transistor 2 of a matrix circuit is separated from a polysilicon thin film 11 by a gate insulating film 14 and an interlayer insulating film 19, while a gate electrode 15 of a NMOS thin film transistor 4 is separated from a polysilicon thin film 12 by only the gate insulating film 14. (See Fig. 1.) While Matsumoto is silent as to the thicknesses of the films 14 and 19, the figures (e.g., Fig. 1) indicate that each of the films 14 and 19 is of roughly the same thickness as the polysilicon films 11 and 12 and the gate electrodes 15 and 20. Thus, using the thicknesses provided by Yamazaki, each of the films 14 and 19 would have a thickness of between is 0.3 mm and 0.7 mm for a combined thickness of between 0.6 mm and 1.4 mm.

In the final action, the Examiner asserts that a person of ordinary skill in the art would have been motivated to combine Yamazaki and Matsumoto in view of Matsumoto's disclosure that the thin film transistor 2, in which the gate electrode 20 is separated from the polysilicon thin film 11 by the combined thickness of the two films 14 and 19, has better operating characteristics than the thin film transistor 4, in which the gate electrode 15 is separated from the polysilicon thin film 11 by the thickness of the film 14.

Assuming for sake of argument that the statements in Matsumoto would have provided motivation to use a thicker gate insulating film, this could have been done in a number of ways: (1) by replacing Yamazaki's thin gate insulating film with the two thicker films described by Matsumoto; (2) by increasing the thickness of Yamazaki's gate insulating film; (3) by adding a second gate insulating film prior to the etching process illustrated by Yamazaki's Fig. 5C; or (4) by adding a second gate insulating film after the etching process illustrated by Yamazaki's Fig. 5C. The first approach would have resulted in an arrangement in which neither film had a side aligned with the side of the semiconductor island, the second approach would have resulted in an arrangement that included only a single gate insulating film, and the third approach would have resulted in an arrangement in which the second insulating film did not extend beyond an edge of the first insulating film. Only the fourth approach would have resulted in the arrangement of insulating films recited in the claims.

If a person of ordinary skill in the art were to modify Yamazaki in order to obtain the benefits of a thicker gate insulating film as described by Matsumoto, the person would have been much more likely to have taken the first approach, which would have used the two thick films of Matsumoto and provided the same combined film thickness (e.g., between 0.6 mm and 1.4 mm) that produced the beneficial results of Matsumoto, than the fourth approach, which would have employed Yamazaki's thin film and only one of Matsumoto's thicker films for a much reduced combined film thickness (e.g., between 0.4 mm and 0.8 mm). (If the thickness of the films could be arbitrarily changed, then the person would have been much more likely to use the second approach than the fourth approach in order to avoid the extraneous step of adding a second layer.) If the person were to depart from Matsumoto's use of two films that cover the entire surface of the chip, then the person would have been much more likely to apply the films prior to the etching process illustrated in Fig. 5C (i.e., to take the third approach) than to apply one before and one after (i.e., to take the fourth approach). Thus, absent impermissible hindsight reconstruction of the invention, the alleged benefits of a thicker gate insulating film would not have led the person to combine Yamazaki and Matsumoto in a manner that produces the subject matter claimed.

The argument presented above was raised in response to the final action. In the advisory action, the Examiner merely states that this argument is not persuasive and repeats the

Examiner's position that Matsumoto would have led one or ordinary skill in the art to add a second layer in order to increase the thickness of the insulating. However, this ignores the reasons, as presented above, that the desire for a thicker insulating film would not have led one or ordinary skill in the art to the claimed subject matter.

For the reasons presented above, appellant requests reversal of the rejection of claims 45-64.

No fee is believed to be due. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 9/18/06

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Claims Appendix

Claims 1-44 (canceled)

Claim 45 (previously presented): A semiconductor device comprising:

a crystalline semiconductor island comprising silicon over a substrate, the crystalline semiconductor island comprising a source region, a drain region and a channel formation region provided between the source and the drain region; and

a gate insulating film comprising a first insulating film over the crystalline semiconductor island and a second insulating film over the first insulating film; and

a gate electrode over the gate insulating film,

wherein the first insulating film has a side aligned with a side of the crystalline semiconductor island, and

wherein the second insulating film extends beyond an edge of the first insulating film.

Claim 46 (previously presented): A semiconductor device comprising:

a crystalline semiconductor island comprising silicon over a substrate, the crystalline semiconductor island comprising a source region, a drain region and a channel formation region provided between the source and the drain region; and

a gate insulating film comprising a first insulating film comprising silicon oxide cover the crystalline semiconductor island and a second insulating film comprising silicon oxide over the first insulating film; and

a gate electrode over the gate insulating film,

wherein the first insulating film has a side aligned with a side of the crystalline semiconductor island, and

wherein the second insulating film extends beyond an edge of the first insulating film.

Claim 47 (previously presented): A semiconductor device comprising:

a crystalline semiconductor island comprising silicon over a substrate, the crystalline semiconductor island comprising a source region, a drain region and a channel formation region provided between the source and the drain region; and

a gate insulating film comprising a first insulating film comprising silicon oxide over the crystalline semiconductor island and a second insulating film comprising silicon nitride over the first insulating film; and

a gate electrode over the gate insulating film,

wherein the first insulating film has a side aligned with a side of the crystalline semiconductor island, and

wherein the second insulating film extends beyond an edge of the first insulating film.

Claim 48 (previously presented): A semiconductor device comprising:

a crystalline semiconductor island comprising silicon over a substrate, the crystalline semiconductor island comprising a source region, a drain region and a channel formation region provided between the source and the drain region; and

a gate insulating film comprising a first insulating film comprising silicon nitride over the crystalline semiconductor island and a second insulating film comprising silicon oxide over the first insulating film; and

a gate electrode over the gate insulating film,

wherein the first insulating film has a side aligned with a side of the crystalline semiconductor island, and

wherein the second insulating film extends beyond an edge of the first insulating film.

Claim 49 (previously presented): A semiconductor device comprising:

a crystalline semiconductor island comprising silicon over a substrate, the crystalline semiconductor island comprising a source region, a drain region and a channel formation region provided between the source and the drain region; and

a gate insulating film comprising a first insulating film comprising silicon nitride over the crystalline semiconductor island and a second insulating film comprising silicon nitride over the first insulating film; and

a gate electrode over the gate insulating film,

wherein the first insulating film has a side aligned with a side of the crystalline semiconductor island, and

wherein the second insulating film extends beyond an edge of the first insulating film.

Claim 50 (previously presented): A semiconductor device according to claim 45, wherein the crystalline semiconductor island is formed by irradiating a laser light through the first insulating film.

Claim 51 (previously presented): A semiconductor device according to claim 46, wherein the crystalline semiconductor island is formed by irradiating a laser light through the first insulating film.

Claim 52 (previously presented): A semiconductor device according to claim 47, wherein the crystalline semiconductor island is formed by irradiating a laser light through the first insulating film.

Claim 53 (previously presented): A semiconductor device according to claim 48, wherein the crystalline semiconductor island is formed by irradiating a laser light through the first insulating film.

Claim 54 (previously presented): A semiconductor device according to claim 49, wherein the crystalline semiconductor island is formed by irradiating a laser light through the first insulating film.

Claim 55 (previously presented): A semiconductor device according to claim 50, wherein the laser light is KrF excimer laser light or XeCl excimer laser light.

Claim 56 (previously presented): A semiconductor device according to claim 51, wherein the laser light is KrF excimer laser light or XeCl excimer laser light.

Claim 57 (previously presented): A semiconductor device according to claim 52, wherein the laser light is KrF excimer laser light or XeCl excimer laser light.

Claim 58 (previously presented): A semiconductor device according to claim 53, wherein the laser light is KrF excimer laser light or XeCl excimer laser light.

Claim 59 (previously presented): A semiconductor device according to claim 54, wherein the laser light is KrF excimer laser light or XeCl excimer laser light.

Claim 60 (previously presented): A semiconductor device according to claim 45, wherein the substrate is a glass substrate.

Claim 61 (previously presented): A semiconductor device according to claim 46, wherein the substrate is a glass substrate.

Claim 62 (previously presented): A semiconductor device according to claim 47, wherein the substrate is a glass substrate.

Claim 63 (previously presented): A semiconductor device according to claim 48, wherein the substrate is a glass substrate.

Claim 64 (previously presented): A semiconductor device according to claim 49, wherein the substrate is a glass substrate.

Evidence Appendix

Related Proceedings Appendix